controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting means;

an ECC block code word recognition sub means in sub means-basis pipeline processing for making said first error detecting sub means, said even-numbered error correction sub means, said even-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means in said system control means recognize that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said ECC-block-basis buffer memory, and further making these same sub means contained in said system control means recognize the ECC blocks and the code words which are to be processed therein.

20. The error correction device of claim 1, 2, 5, 6, 7, or 8 wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block recognition sub means for recognizing a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; for recognizing the error correction done by said error correcting means; for recognizing writing of error-corrected data to said plural-ECC-block-division buffer memory by said bus control means; for recognizing ECC blocks in process when said error detecting means stores mid-term results to said plural-ECC-block-division storing means, and for selecting ECC blocks to be processed; and

a collective-type ECC block notification sub means in sub means-basis

pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively transmitted downstream and new ECC blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

21. The error correction device of claim 9 wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;